

Docket No. 01207P008C5

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:

Pani, et al.

Application No: Not yet assigned

Filed: Herewith

For: Method and Apparatus for Universal
Program Controlled Bus Architecture

A Continuation of

Application No. 10/412,975

Filed: April 11, 2003

Examiner: Not yet assigned

Art Unit: Not yet assigned

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicants.

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Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

 X 37 C.F.R. §1.97(b).

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 A statement pursuant to 37 C.F.R. §1.97(e) or

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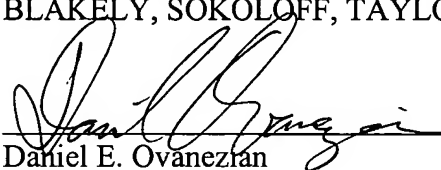
Pursuant to 37 C.F.R. §1.98(d), copies of cited art are not enclosed. The cited art has been previously cited in parent application no. 10/412,975, filed April 11, 2003.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 3/25, 2004


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	First Named Inventor: Peter M. Pani	
	Filing Date: Herewith	

U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Code ²	Kind (If known)			
		4,020,469		Manning	4/26/77	
		4,661,901		Veneski	4/28/87	
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		4,992,680		Benedetti et al.	2/12/91	
		5,144,166		Camarota et al.	9/1/92	
		5,204,556		Shankar	4/20/93	
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		5,825,202		Tavana et al.	10/20/98	
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		Office ³	Number ⁴	Kind Code ⁵ (If known)				
		EP	0415542A1		Advanced Micro Devices, Inc.	3/6/91		
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		GB	2180382A		Pilkington Micro-Electronics Limited	3/25/87		
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		PCT	WO92/08286		Concurrent Logic, Inc.	5/14/92		
		PCT	WO94/28475		Regents of the University of California	12/8/94		
		PCT	WO96/05964		Minnesota Mining and Manufacturing Co.	2/29/96		
		PCT	WO96/35261		BTR, Inc.	11/7/96		
		PCT	WO94/10754		Xilinx, Inc.	5/11/94		
		PCT	WO95/04404		Advantage Logic, Inc.	2/9/95		

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OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
		Richard Cliff et al., "A Dual Granularity and Globally Interconnected Architecture for a Programmable Logic Device", Proceedings of the IEEE 1993 Custom Integrated Circuits Conference, May 1993, pp. 7.3.1-7.3.5.	
		Altera Corporation, Data Sheet, "Flex EPF81188 12,000-Gate Programmable Logic Device", September 1992, Version 1.	
		Minnick, R.C., "A Survey of Microcellular Research", Journal of the Association for Computing Machinery", Vol. 14, No. 2, April 1967, pp. 203-241.	
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		Ping-Tsung Wang et al., "A High Performance FPGA with Hierarchical Interconnection Structure", Institute of Electrical and Electronic Engineers, pp. 239-242, May 30, 1994.	
		Motorola Product Brief, "MPA10XX Field Programmable Gate Arrays", 4 pages total, September 27, 1993.	
		Krambeck, R.H. "ORCA: A High Performance, Easy to Use SRAM Based Architecture", Wescon '93 record, pp. 310-320, September 20-30, 1993.	
		Buffoli et al., "Dynamically Reconfigurable Devices used to Implement a Self-Tuning, High Performance PID Controller", IEEE 1989, pp. 107-112.	
		Devadas, S., "Boolean Decomposition of Programmable Logic Arrays", IEEE 1988, pp. 2.5.1-2.5.5.	

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		Vidal, J., "Implementing Neural Nets with Programmable Logic", IEEE 1988, pp. 50-53.	
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		Atmel Corporation, "Field Programmable Gate Arrays – AT6000 Series", 1993.	
		Sinan Kaptanoglu et al., "A New High Density and Very Low Cost Reprogrammable FPGA Architecture", 10 pages.	
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		F. Zlotnick et al., "A High Performance Fine-Grained Approach to SRAM based FPGAs, Wescon '93 Record, pp. 321-326, September 28-30, 1993.	
		Barry K. Britton et al., "Optimized Reconfigurable Cell Array Architecture for High Performance Field Programmable Gate Arrays", Proceedings of the IEEE 1993 Custom Integrated Circuits Conference, May 1993, pp. 7.2.1-7.2.5.	

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